



[illegible][illegible]6C  
IT8900  
0000[illegible]

**Design SP Source:**

[illegible][illegible]

PPE Requirements	
Wear	Hard hat
Wear	
Wear	
Wear	
Wear	Eye protection
Wear	Ear protection
Wear	Hand protection
Wear	Foot protection
Wear	Respiratory protection
Wear	Protective clothing

Week	Topic
Week 1	Introduction to the course
Week 2	Basic concepts of statistics
Week 3	Descriptive statistics
Week 4	Inferential statistics
Week 5	Regression analysis
Week 6	ANOVA
Week 7	Non-parametric tests
Week 8	Bayesian statistics
Week 9	Advanced topics
Week 10	Final exam


Year	Population	Population	Population
1990	100	100	100
2000	100	100	100
2010	100	100	100
2020	100	100	100
2030	100	100	100
2040	100	100	100
2050	100	100	100
2060	100	100	100
2070	100	100	100
2080	100	100	100
2090	100	100	100
2100	100	100	100

	SBB 12-2-Steel	20
	SBB 12-2-Ty	20
	SBB 12-2-Ty	20
	SBB 12-2	

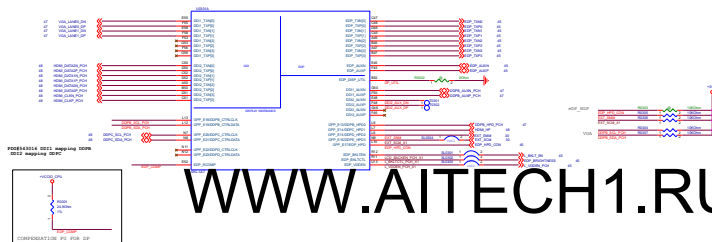
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Display Port

A	DDP
B	VGA
C	DDMI

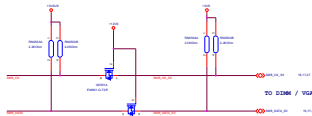
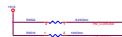
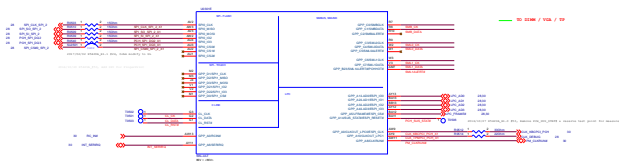
Intel Version	ASUS P/N
pcw-42	



ASUS	Project Name	Rev
X5430A/UV		Rev
Title :	zhc_wenku	
Dept :	MSI,MSI,MSI	Engineer :
Design :	MSI,MSI,MSI	MSI,MSI,MSI

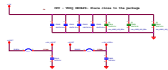
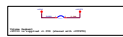
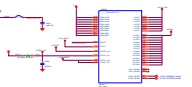






WWW.AITECH1.RU





Sealing guidelines for MINIKIT placement for 400, 450 & 500

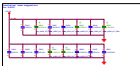
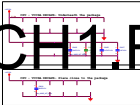


Reading position for EBLIFE placement for 2000: 22.5%

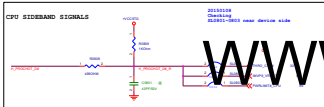


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Index	Sub-Index	Index	Sub-Index
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16
17	17	17	17
18	18	18	18
19	19	19	19
20	20	20	20
21	21	21	21
22	22	22	22
23	23	23	23
24	24	24	24
25	25	25	25
26	26	26	26
27	27	27	27
28	28	28	28
29	29	29	29
30	30	30	30
31	31	31	31
32	32	32	32
33	33	33	33
34	34	34	34
35	35	35	35
36	36	36	36
37	37	37	37
38	38	38	38
39	39	39	39
40	40	40	40
41	41	41	41
42	42	42	42
43	43	43	43
44	44	44	44
45	45	45	45
46	46	46	46
47	47	47	47
48	48	48	48
49	49	49	49
50	50	50	50
51	51	51	51
52	52	52	52
53	53	53	53
54	54	54	54
55	55	55	55
56	56	56	56
57	57	57	57
58	58	58	58
59	59	59	59
60	60	60	60
61	61	61	61
62	62	62	62
63	63	63	63
64	64	64	64
65	65	65	65
66	66	66	66
67	67	67	67
68	68	68	68
69	69	69	69
70	70	70	70
71	71	71	71
72	72	72	72
73	73	73	73
74	74	74	74
75	75	75	75
76	76	76	76
77	77	77	77
78	78	78	78
79	79	79	79
80	80	80	80
81	81	81	81
82	82	82	82
83	83	83	83
84	84	84	84
85	85	85	85
86	86	86	86
87	87	87	87
88	88	88	88
89	89	89	89
90	90	90	90
91	91	91	91
92	92	92	92
93	93	93	93
94	94	94	94
95	95	95	95
96	96	96	96
97	97	97	97
98	98	98	98
99	99	99	99

[illegible]

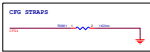
## Main Board



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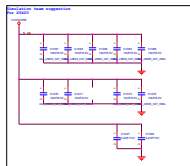
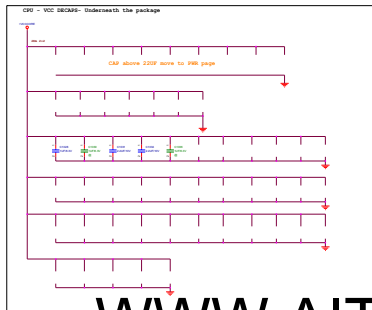
		Project Name		Rev
<b>XS42UA/UV</b>				10.0
Title : CPU_MISC.ITAG.CLK				
Date	Dept.		Engineer	
6	H&D_RnE_E&I		Joach_Wang	
Code	Creating	date	10/2/2017	

### Main Board



	1	0	NOTE
CPUS	NO STALL	STALL	STALL REENT SEQUENCE AFTER PC0 FULL LOCK UNTIL DE-ASSERTED
CPUS	DISTANCE	BRANCH	NO BRANCH



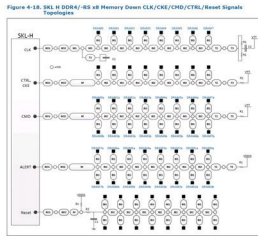


REVISION HISTORY

REV	DESCRIPTION	DATE	BY
C1072	Remove		
C1037	Add	add 0402	2.2uF
C1038	Add	add 0402	2.2uF
C1031	1uF to 2.2uF	convert to 2.2uF	
C1034	1uF to 2.2uF	convert to 2.2uF	

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CC/USB++ 140804

Intel Confidential

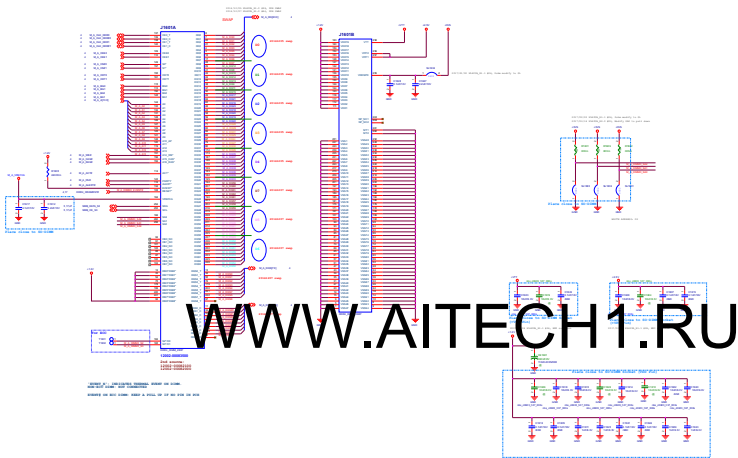
123

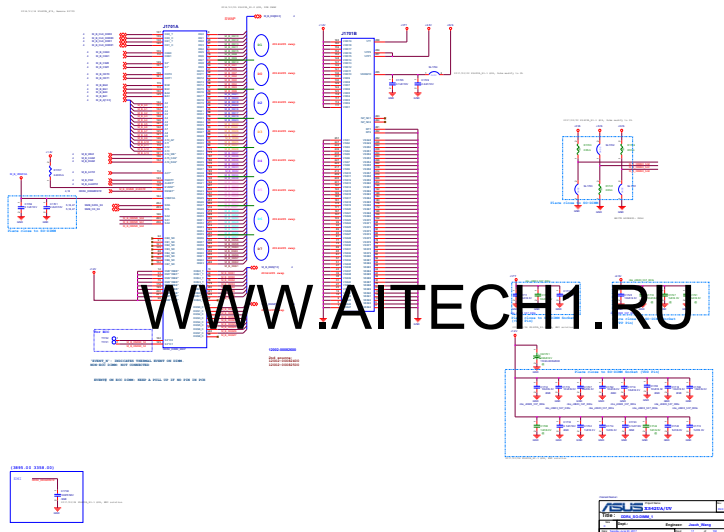
Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS 80-GB/s ECC	DDR4/-RS 80-GB/s no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)
Control	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)	CS#(1:0), CS#(3:2), CS#(5:4), CS#(7:6)
Command (C#)	RA[0], RA[1], RA[2], RA[3], RA[4], RA[5], RA[6], RA[7]	RA[0], RA[1], RA[2], RA[3], RA[4], RA[5], RA[6], RA[7]	RA[0], RA[1], RA[2], RA[3], RA[4], RA[5], RA[6], RA[7]	CAH[0], CAH[1], CAH[2], CAH[3], CAH[4], CAH[5], CAH[6], CAH[7]
Strobe	DQS#(7:0), DQS#(15:8), DQS#(23:16), DQS#(31:24)	DQS#(7:0), DQS#(15:8), DQS#(23:16), DQS#(31:24)	DQS#(7:0), DQS#(15:8), DQS#(23:16), DQS#(31:24)	DQS#(7:0), DQS#(15:8), DQS#(23:16), DQS#(31:24)
ECC strobe	DQS#(7:0), DQS#(15:8), DQS#(23:16), DQS#(31:24)	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	SRAM_RESET#	SRAM_RESET#	SRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

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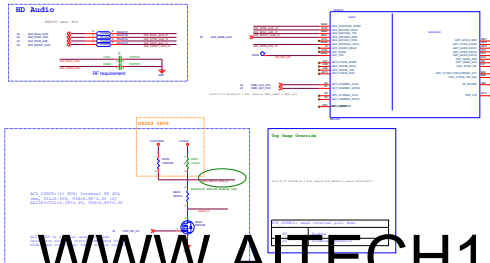






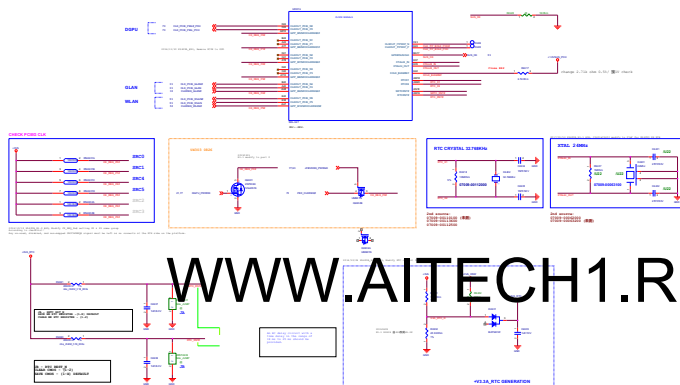


ACE SCIX ADD and ACE SDOOT ADD  
Total TxRx match < 500 mV



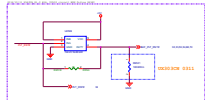
WWW.AITECH1.RU



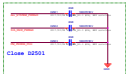


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Main Board

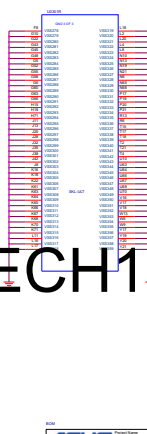
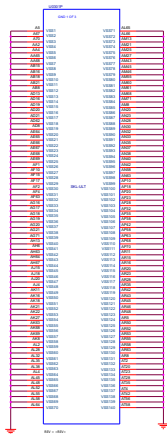


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ASUS Project Name: X542UA/UV

Rev: 01.0

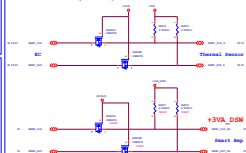
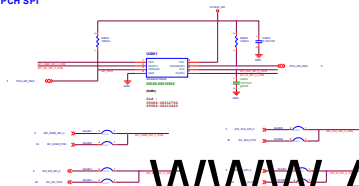
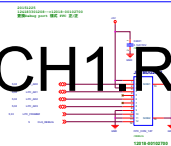
File: CPU\_FCH\_POWER.DWG

Dept: H&M\_MFG\_P01 Engineer: Joesch\_Wang

Date: Tuesday, June 20, 2017 Time: 07:47 of 100

### SPI PCH Power

The diagram illustrates the SPI PCH Power circuit. It features a MOSFET with its gate connected to the SPI PCH Power signal. The drain is connected to the VDDIO\_1V8 supply, and the source is connected to ground (GND). A diode is connected in parallel with the MOSFET, with its cathode towards the drain. The MOSFET is also connected to VDDIO\_1V8 and GND through a network of resistors and capacitors, including a 10k resistor and a 100nF capacitor.

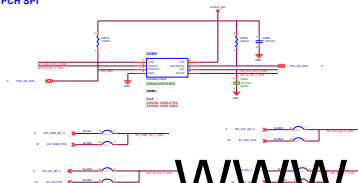
[illegible][illegible]

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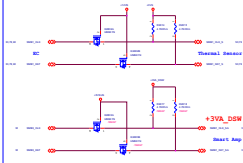
## SPI PCH Power



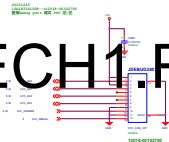
## 2nd PCH SPI



## System Management Interface



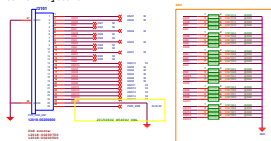
LPC Debug Port



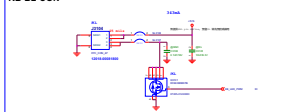
WWW.AITECH1.RU



# Internal Keyboard



# KB BL CON

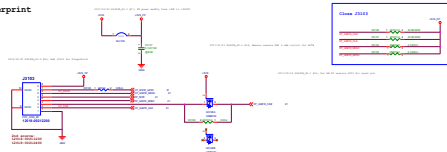


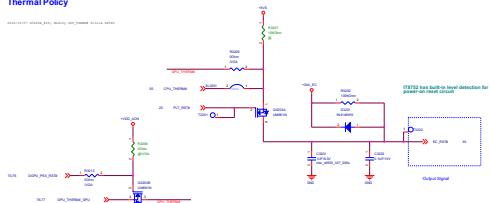
# Touch PAD



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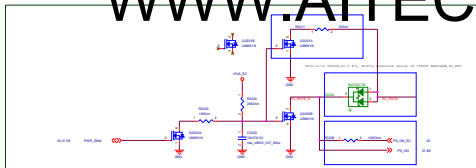
# Fingerprint





battery embedded (press down, say 10 sec, then reset etc.)

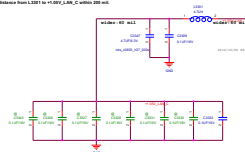
WWW.AITECH1.RU



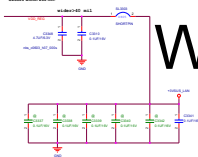
ASUS		Project Name		Rev	
Title : <u>XS420A/UV</u>				Rev	
Date : <u>2012-07-20</u>		Dept. : <u>MSD_MCU_DSI</u>		Engineer : <u>Joach_Wang</u>	
Date : <u>2012-07-20</u>		Drawn : <u>Joach_Wang</u>		Rev : <u>1.0</u>	

The distance from u3201.26 to L3201 within 200 mil.

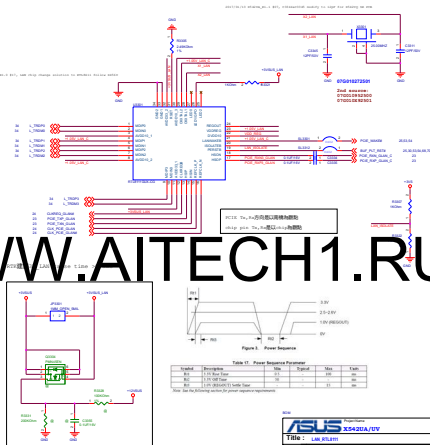
The distance from L3201 to +5.0V\_LAN\_C within 200 mil.



The distance from U3201.24, U3201.25, V320\_HSD out to L3201 within 200 mil.



avoid/leave vias, pins, vias, keep chip change resistance to avoid/leave vias



PCIE Tx, Rx 50 ohm 以网络为限制  
usb, pci, SATA 以 50 ohm 为限制

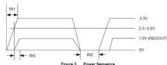


Figure 3. Power Sequence

Table 11. Power Sequence Parameter

Symbol	Description	Min	Typ	Max	Units
R1	1.0V Rise Time	10	—	100	ns
R2	1.0V Fall Time	10	—	100	ns
R3	1.0V (PS0V0V) to 1.0V (PS0V0V) Setup Time	10	—	10	ns

Note: See the following section for power sequence requirements.

ASUS X542VA/UV

Title: L3201

Rev: 1.0

Proj: 100-001-001

Engineer: Jiaoh\_Wang

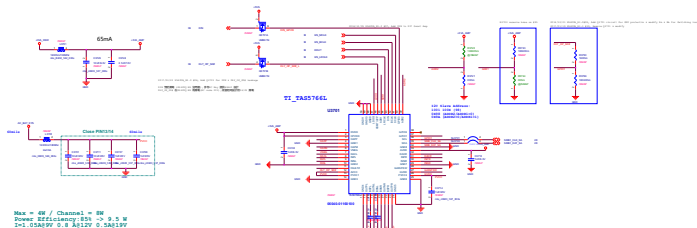
Rev: 1.0







# SMART AMP. & SPK



# WWW.AITECH1.RU

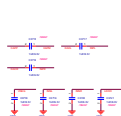
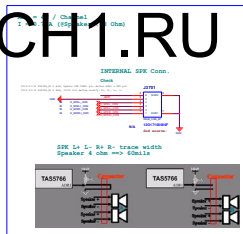
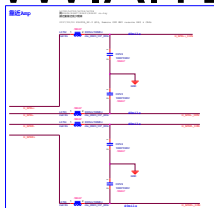


Table 11. Gain and PSRR

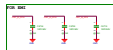
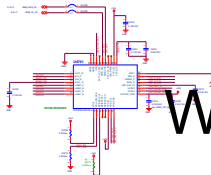
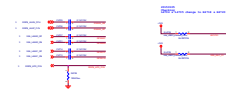
f <sub>in</sub> (Hz)	P <sub>in</sub> (dBm)	P <sub>out</sub> (dBm)	PSRR (dB)	f <sub>in</sub> (Hz)	P <sub>in</sub> (dBm)	P <sub>out</sub> (dBm)	PSRR (dB)
10	10	10	10	10	10	10	10
100	10	10	10	100	10	10	10
1000	10	10	10	1000	10	10	10
10000	10	10	10	10000	10	10	10
100000	10	10	10	100000	10	10	10





## eDP to VGA

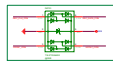
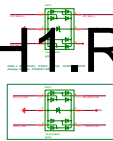
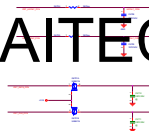
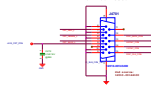
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## CRT D-SUB



### CRT Connector



Legend:

- 1. CRT\_DSUB\_0
- 2. CRT\_DSUB\_1
- 3. CRT\_DSUB\_2
- 4. CRT\_DSUB\_3
- 5. CRT\_DSUB\_4
- 6. CRT\_DSUB\_5



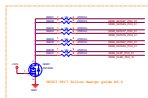
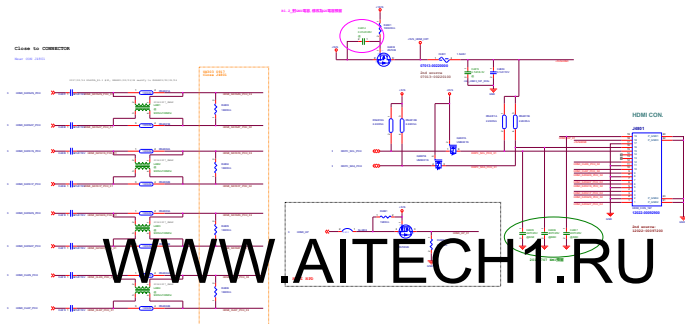
Legend:

- 1. CRT\_DSUB\_0
- 2. CRT\_DSUB\_1
- 3. CRT\_DSUB\_2
- 4. CRT\_DSUB\_3
- 5. CRT\_DSUB\_4
- 6. CRT\_DSUB\_5



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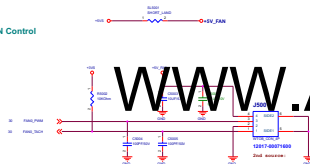
# HDMI type-A



## CPU Thermal Sensor



## DC FAN Control



請將測試至於FAN座  
B2.0 8pin\_fan\_20150820

## 5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000b (x is RW bit).

## 5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)	
ALERT	2KΩ	75	
	7.5KΩ	90	
	10.5KΩ	100	
	14KΩ	105	
	16.7KΩ	110	

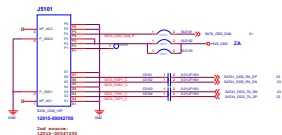
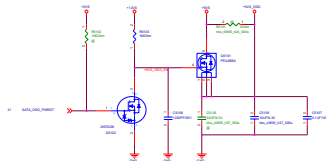
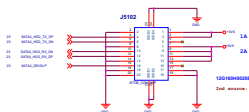
Route CPU\_THRM\_DA , CPU\_THRM\_DC and on the same layer

OTHER SIGNALS  
10 mils  
-----GND  
10 mils  
-----THERMDA(10 mils)  
10 mils  
-----THERMDC(10 mils)  
10 mils  
-----GND  
10 mils  
-----OTHER SIGNALS  
Avoid FSB Power

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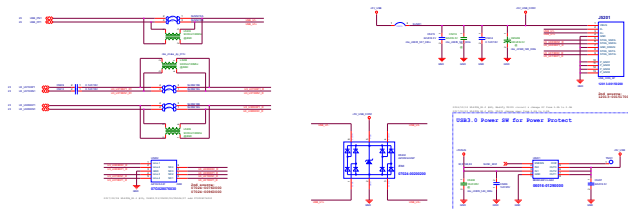
Customer Name		Project Name	
TSS		X5420A/UV	
Date		Rev	
By		Engineer	
Date		Date	

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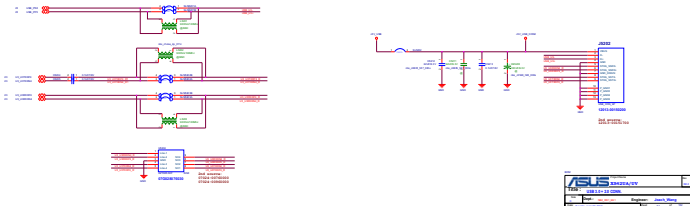
[illegible]

		Project Name		Rev	
		X542UA/UV		Rev 0	
Title : SATA000					
Rev		Dept.: HSE_HCI_001		Engineer: Jason_Wang	
Date		Created		Drawn	
2016-09-06 10:24:17		2016-09-06 10:24:17		2016-09-06 10:24:17	

USB3.0\_Port 0



USB3.0\_Port 1



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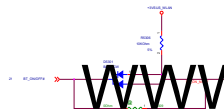


## WLAN CONN.

000000000 WLAN\_PU\_0 BTL: Please refer to the following circuit



000000000 WLAN\_PU\_0 BTL: Please refer to the following circuit

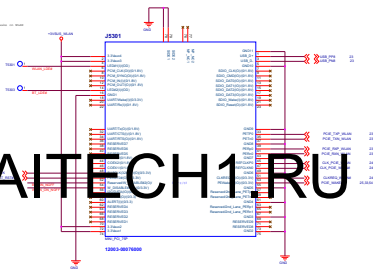


000000000 WLAN\_PU\_0 BTL: Please refer to the following circuit

000000000 WLAN\_PU\_0 BTL: Please refer to the following circuit

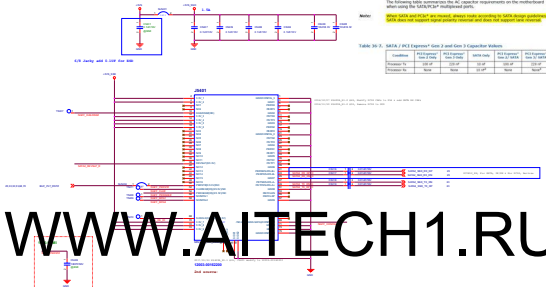
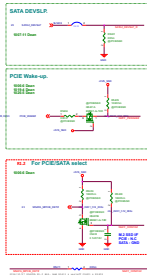


000000000 WLAN\_PU\_0 BTL: Please refer to the following circuit



Product Name		Project Name		Rev	
		XS420A/UV		R0.0	
Title :		MINICARD(WLAN)			
Dept. :		WLAN		Engineer: Jiawen Wang	
Rev. :		1.0		Rev. :	
Date: Tuesday, June 20, 2017		Drawn: JZ		By: JZ	

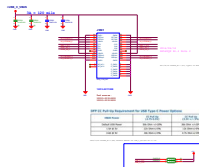
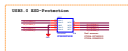
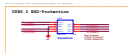
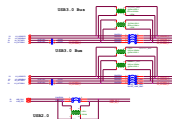
Main Board



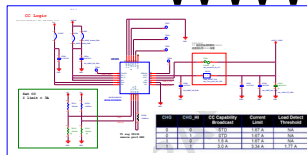
WWW.AITECH1.RU

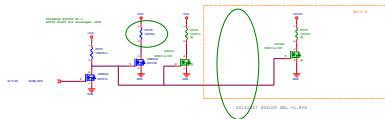
## USB 3.0 TypeC CONN.

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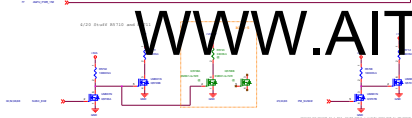
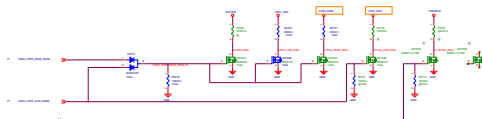


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Main Board

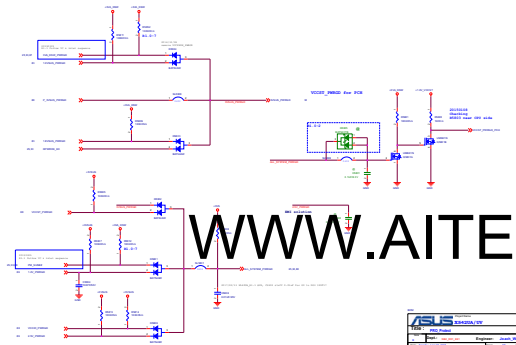


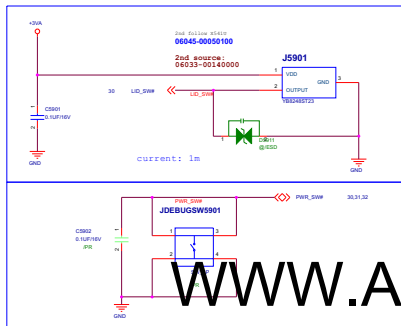
WWW.AITECH1.RU



ASUS		Model: K4000/REY	Rev: 1.0
Title: 100 Base-T		Author: Andy Tang	Rev: 1.0
Date: 2015.07.07		Rev: 1.0	Rev: 1.0

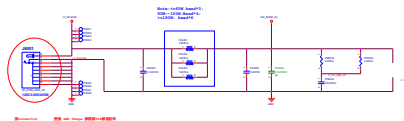
Main Board



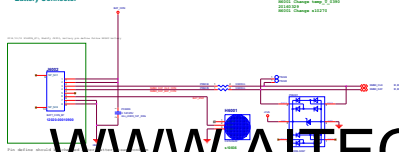


<Variant Name>

ASUS		Project Name	Rev
X5420A/UV			V0.0
Title : SR_Power & WiFi & CAP LED			
Size	Dept.:	Engineer:	
A	NEO_R01_001	Joach_Wang	
Date	Tuesday, June 20, 2017	Sheet	59 of 102



Battery Connector



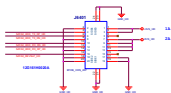
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X540 電池 connector pin define  
(Pin 定義)

Pin No.	Signal	Description	Remark
1	P+	Battery pack positive terminal	Output voltage
2	P+	Battery pack positive terminal	Output voltage
3	SMBC	Serial clock input	SMBC
4	SMBD	Serial data input	SMBD
5	NC		
6	ENB	External charge & discharge Monitor control pin	
7	P-	Battery pack negative terminal	GND
8	P-	Battery pack negative terminal	GND



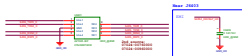
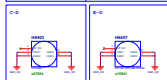
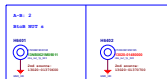
**SATA HDD BtoB CONN.**



**SATA HDD CONN.**



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# DB\_IO

DB\_IO is a module that provides a connection between the DB and the IO. It is used to connect the DB to the IO and to provide a connection between the DB and the IO.

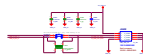
## HDD DB to IO DB FPC CONN.

Hardware connection between the HDD DB and the IO DB FPC CONN. The connection is made by using the FPC CONN. The connection is made by using the FPC CONN. The connection is made by using the FPC CONN.

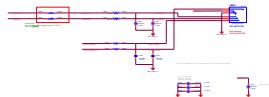


# USB 2.0 con.

USB 2.0 con. is a module that provides a connection between the USB 2.0 and the IO. It is used to connect the USB 2.0 to the IO and to provide a connection between the USB 2.0 and the IO.



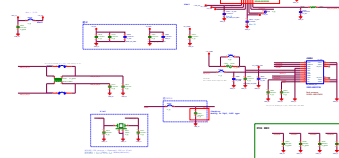
# AUDIO JACK



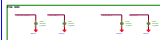
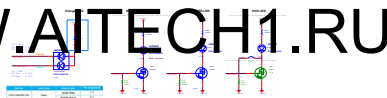
# SD Card Reader

Signal	IO	IO	IO
Card detect	IO1	IO2	IO3
Card data	IO4	IO5	IO6
Card clock	IO7	IO8	IO9
Card power	IO10	IO11	IO12

SD Card Reader is a module that provides a connection between the SD Card and the IO. It is used to connect the SD Card to the IO and to provide a connection between the SD Card and the IO.

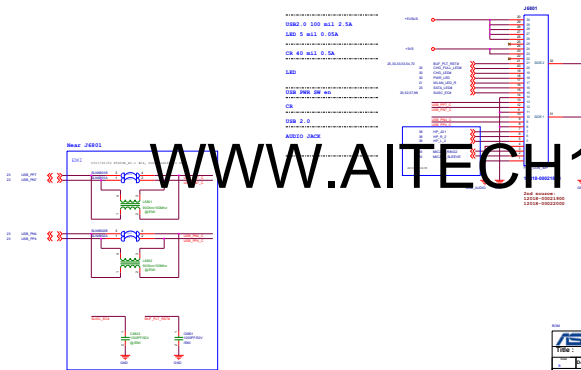


# LED indicator



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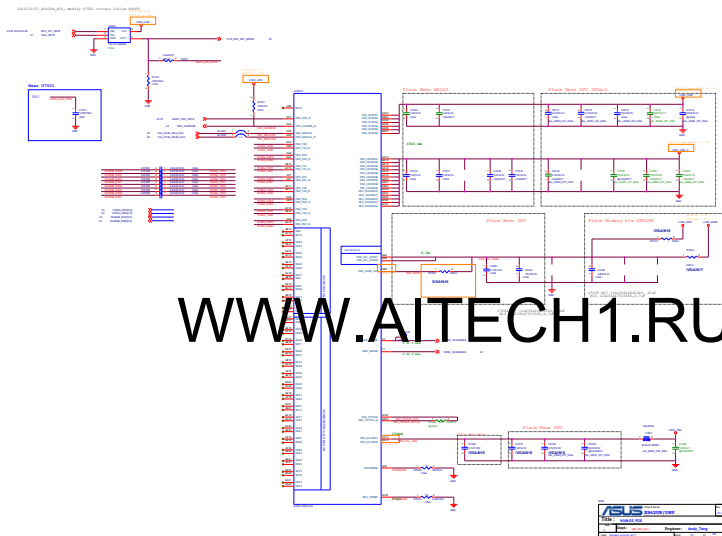
**MB to IO DB FPC CONN.**

[illegible]

8C30

		Project Name		Rev
<b>Title :</b> <b>8TO8 CONNECTOR</b>		<b>X542UQ/UV</b>		<b>Rev.0</b>
<b>Dept.:</b> <b>MOB_A02_001</b>	<b>Engineer:</b> <b>Joach_Wang</b>			
Date: <b>2016.02.02</b>	Drawn: <b>00</b>	Check: <b>00</b>	App: <b>100</b>	







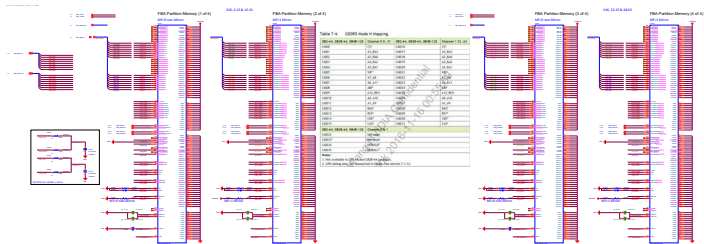


Table 7-14. GDDR6 Mode H Mapping

Configuration	Requirements	Notes
1	Memory bank 0 must be used for memory bank 1.	
2	Memory bank 1 must be used for memory bank 2.	
3	Memory bank 2 must be used for memory bank 3.	
4	Memory bank 3 must be used for memory bank 4.	

7.1.12.1 VSP-D

VSP-D connections for i76 mode.

7.1.12.2 VSP-C

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

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VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

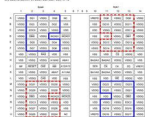
VSP-C connections for i76 mode.

VSP-C connections for i76 mode.

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Figure 7-14. VSP-C Connections for i76 Mode

5.1.12.12.1 VSP-D



5.1.12.12.2 VSP-C

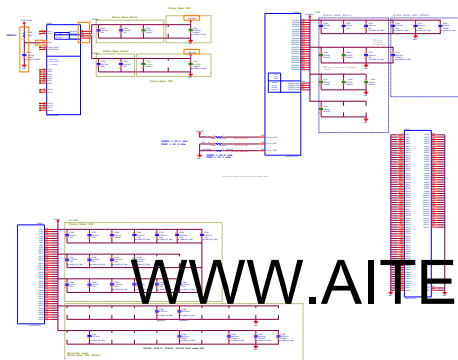


5.1.12.12.3 VSP-D

Configuration	Requirements	Notes
1	Memory bank 0 must be used for memory bank 1.	
2	Memory bank 1 must be used for memory bank 2.	
3	Memory bank 2 must be used for memory bank 3.	
4	Memory bank 3 must be used for memory bank 4.	



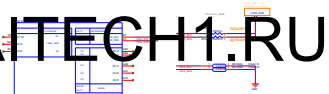
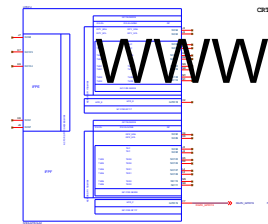
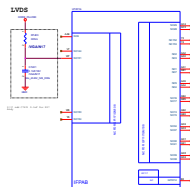
5.1.12.12.4 VSP-C



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Table 10. Winbond 64Tbit 64Tbit Straps

Strap No.	Strap Configuration	Comment
W0A_00	W0A_00[0:15]	W0A_00[0:15] = 0x00000000
W0A_01	W0A_01[0:15]	W0A_01[0:15] = 0x00000000
W0A_02	W0A_02[0:15]	W0A_02[0:15] = 0x00000000
W0A_03	W0A_03[0:15]	W0A_03[0:15] = 0x00000000
W0A_04	W0A_04[0:15]	W0A_04[0:15] = 0x00000000
W0A_05	W0A_05[0:15]	W0A_05[0:15] = 0x00000000
W0A_06	W0A_06[0:15]	W0A_06[0:15] = 0x00000000
W0A_07	W0A_07[0:15]	W0A_07[0:15] = 0x00000000
W0A_08	W0A_08[0:15]	W0A_08[0:15] = 0x00000000
W0A_09	W0A_09[0:15]	W0A_09[0:15] = 0x00000000
W0A_10	W0A_10[0:15]	W0A_10[0:15] = 0x00000000
W0A_11	W0A_11[0:15]	W0A_11[0:15] = 0x00000000
W0A_12	W0A_12[0:15]	W0A_12[0:15] = 0x00000000
W0A_13	W0A_13[0:15]	W0A_13[0:15] = 0x00000000
W0A_14	W0A_14[0:15]	W0A_14[0:15] = 0x00000000
W0A_15	W0A_15[0:15]	W0A_15[0:15] = 0x00000000

Table 10-2. Resistance Mapping for New Values

Resistance Value	Mapping to W0A_00	Mapping to W0A_01
100 Ohm	0x00000000	0x00000000
120 Ohm	0x00000001	0x00000001
150 Ohm	0x00000002	0x00000002
180 Ohm	0x00000003	0x00000003
220 Ohm	0x00000004	0x00000004
270 Ohm	0x00000005	0x00000005
330 Ohm	0x00000006	0x00000006
400 Ohm	0x00000007	0x00000007
470 Ohm	0x00000008	0x00000008
560 Ohm	0x00000009	0x00000009
680 Ohm	0x0000000A	0x0000000A
820 Ohm	0x0000000B	0x0000000B
1000 Ohm	0x0000000C	0x0000000C
1200 Ohm	0x0000000D	0x0000000D
1500 Ohm	0x0000000E	0x0000000E
1800 Ohm	0x0000000F	0x0000000F

Strap No.	Strap Configuration	Comment
W0A_16	W0A_16[0:15]	W0A_16[0:15] = 0x00000000
W0A_17	W0A_17[0:15]	W0A_17[0:15] = 0x00000000
W0A_18	W0A_18[0:15]	W0A_18[0:15] = 0x00000000
W0A_19	W0A_19[0:15]	W0A_19[0:15] = 0x00000000
W0A_20	W0A_20[0:15]	W0A_20[0:15] = 0x00000000
W0A_21	W0A_21[0:15]	W0A_21[0:15] = 0x00000000
W0A_22	W0A_22[0:15]	W0A_22[0:15] = 0x00000000
W0A_23	W0A_23[0:15]	W0A_23[0:15] = 0x00000000
W0A_24	W0A_24[0:15]	W0A_24[0:15] = 0x00000000
W0A_25	W0A_25[0:15]	W0A_25[0:15] = 0x00000000
W0A_26	W0A_26[0:15]	W0A_26[0:15] = 0x00000000
W0A_27	W0A_27[0:15]	W0A_27[0:15] = 0x00000000
W0A_28	W0A_28[0:15]	W0A_28[0:15] = 0x00000000
W0A_29	W0A_29[0:15]	W0A_29[0:15] = 0x00000000
W0A_30	W0A_30[0:15]	W0A_30[0:15] = 0x00000000
W0A_31	W0A_31[0:15]	W0A_31[0:15] = 0x00000000

Table 11. Winbond 64Tbit Straps

Strap No.	Strap Configuration	Comment
W0A_32	W0A_32[0:15]	W0A_32[0:15] = 0x00000000
W0A_33	W0A_33[0:15]	W0A_33[0:15] = 0x00000000
W0A_34	W0A_34[0:15]	W0A_34[0:15] = 0x00000000
W0A_35	W0A_35[0:15]	W0A_35[0:15] = 0x00000000
W0A_36	W0A_36[0:15]	W0A_36[0:15] = 0x00000000
W0A_37	W0A_37[0:15]	W0A_37[0:15] = 0x00000000
W0A_38	W0A_38[0:15]	W0A_38[0:15] = 0x00000000
W0A_39	W0A_39[0:15]	W0A_39[0:15] = 0x00000000
W0A_40	W0A_40[0:15]	W0A_40[0:15] = 0x00000000
W0A_41	W0A_41[0:15]	W0A_41[0:15] = 0x00000000
W0A_42	W0A_42[0:15]	W0A_42[0:15] = 0x00000000
W0A_43	W0A_43[0:15]	W0A_43[0:15] = 0x00000000
W0A_44	W0A_44[0:15]	W0A_44[0:15] = 0x00000000
W0A_45	W0A_45[0:15]	W0A_45[0:15] = 0x00000000
W0A_46	W0A_46[0:15]	W0A_46[0:15] = 0x00000000
W0A_47	W0A_47[0:15]	W0A_47[0:15] = 0x00000000
W0A_48	W0A_48[0:15]	W0A_48[0:15] = 0x00000000
W0A_49	W0A_49[0:15]	W0A_49[0:15] = 0x00000000
W0A_50	W0A_50[0:15]	W0A_50[0:15] = 0x00000000
W0A_51	W0A_51[0:15]	W0A_51[0:15] = 0x00000000

Table 11-2. Resistance Mapping for New Values

Resistance Value	Mapping to W0A_32	Mapping to W0A_33
100 Ohm	0x00000000	0x00000000
120 Ohm	0x00000001	0x00000001
150 Ohm	0x00000002	0x00000002
180 Ohm	0x00000003	0x00000003
220 Ohm	0x00000004	0x00000004
270 Ohm	0x00000005	0x00000005
330 Ohm	0x00000006	0x00000006
400 Ohm	0x00000007	0x00000007
470 Ohm	0x00000008	0x00000008
560 Ohm	0x00000009	0x00000009
680 Ohm	0x0000000A	0x0000000A
820 Ohm	0x0000000B	0x0000000B
1000 Ohm	0x0000000C	0x0000000C
1200 Ohm	0x0000000D	0x0000000D
1500 Ohm	0x0000000E	0x0000000E
1800 Ohm	0x0000000F	0x0000000F

Table 11-3. Resistance Mapping for New Values

Resistance Value	Mapping to W0A_32	Mapping to W0A_33
100 Ohm	0x00000000	0x00000000
120 Ohm	0x00000001	0x00000001
150 Ohm	0x00000002	0x00000002
180 Ohm	0x00000003	0x00000003
220 Ohm	0x00000004	0x00000004
270 Ohm	0x00000005	0x00000005
330 Ohm	0x00000006	0x00000006
400 Ohm	0x00000007	0x00000007
470 Ohm	0x00000008	0x00000008
560 Ohm	0x00000009	0x00000009
680 Ohm	0x0000000A	0x0000000A
820 Ohm	0x0000000B	0x0000000B
1000 Ohm	0x0000000C	0x0000000C
1200 Ohm	0x0000000D	0x0000000D
1500 Ohm	0x0000000E	0x0000000E
1800 Ohm	0x0000000F	0x0000000F

Table 11-4. Resistance Mapping for New Values

Resistance Value	Mapping to W0A_32	Mapping to W0A_33
100 Ohm	0x00000000	0x00000000
120 Ohm	0x00000001	0x00000001
150 Ohm	0x00000002	0x00000002
180 Ohm	0x00000003	0x00000003
220 Ohm	0x00000004	0x00000004
270 Ohm	0x00000005	0x00000005
330 Ohm	0x00000006	0x00000006
400 Ohm	0x00000007	0x00000007
470 Ohm	0x00000008	0x00000008
560 Ohm	0x00000009	0x00000009
680 Ohm	0x0000000A	0x0000000A
820 Ohm	0x0000000B	0x0000000B
1000 Ohm	0x0000000C	0x0000000C
1200 Ohm	0x0000000D	0x0000000D
1500 Ohm	0x0000000E	0x0000000E
1800 Ohm	0x0000000F	0x0000000F

WWW.AITECH1.RU

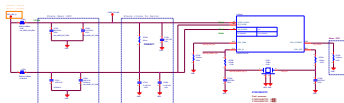
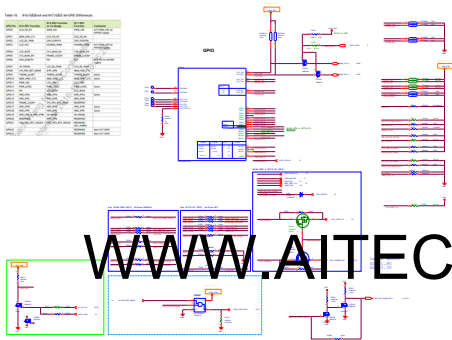
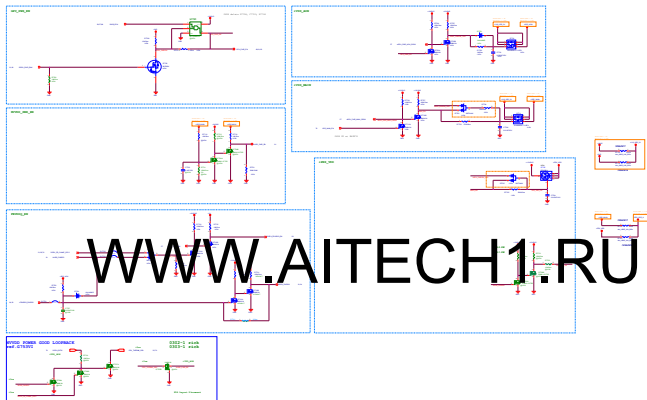
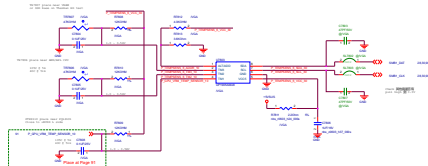


Table 15.  $\text{WR}_{\text{C}}(\text{DB-44})$  and  $\text{WR}_{\text{C}}(\text{DB-44})/(\text{DB-44})$  Difference.[illegible]

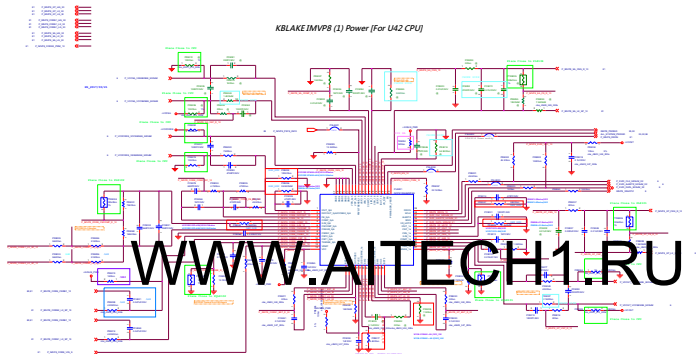


WWW.AITECH1.RU

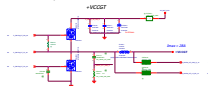


[illegible]

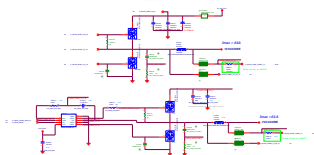
WWW.AITECH1.RU



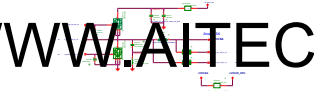
SkyLake-BNVP8 Power (2) (For CPU)



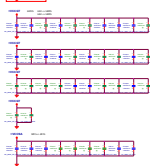
+VCCCORE



+VCCSA



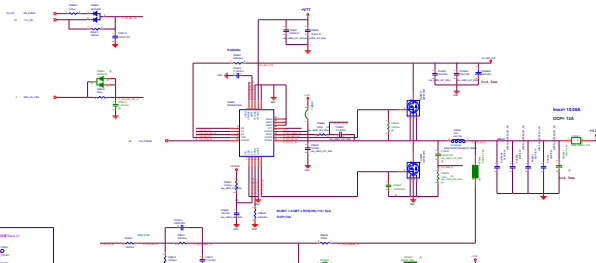
WWW.AITECH1.RU





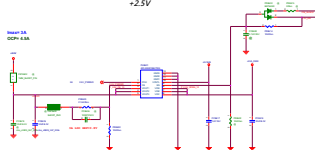


+1.2V / +VTT / +2.5V[For Memory]

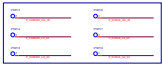


WWW.AITECH1.RU

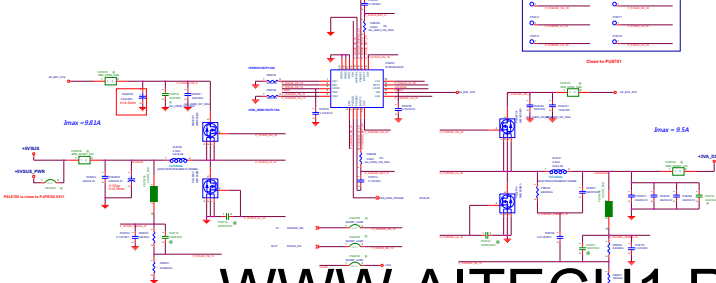
+2.5V



+3VA\_DSW / +5VSUS [System Power]



**Close to POSTS:**



WWW.AITECH1.RU

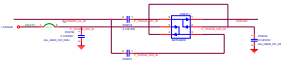


圖 3 的電阻值: +12V 和 5V 的電阻對地電阻不應小於 10kΩ。

Adaptive Works (2014)

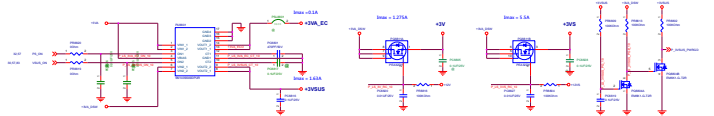
	50	55	60	65	70	75	Anzahl nicht-überzeugter
PIG_50	5	—	5	—	5	—	5
IGIG_55_50	5	—	5	—	5	—	5
IGIG_60_50	5	—	5	—	5	—	5
IGIG_65_50	5	—	5	—	5	—	5
IGIG_70_50	5	—	5	—	5	—	5
IGIG_75_50	5	—	5	—	5	—	5
IGIG_55_60	5	—	5	—	5	—	5
IGIG_60_60	5	—	5	—	5	—	5

Bathory Media (P/W/P)

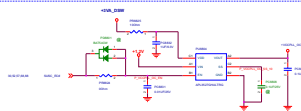
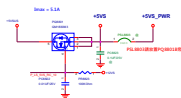
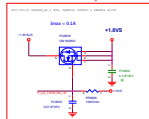
	50	175	500	1000	5000	10000	100000 with change?
one_job	1	-	-	1	0	0	0
fourteen_job	1	-	-	0	0	0	0
fortyjob_job	1	-	-	0	0	0	0
fortyjob_job	1	-	-	0	0	0	1
10000_job	1	-	-	0	0	0	0
tenjob_job	1	-	-	0	0	0	0
tenjob_job	1	-	-	0	0	0	0



# Load Switch



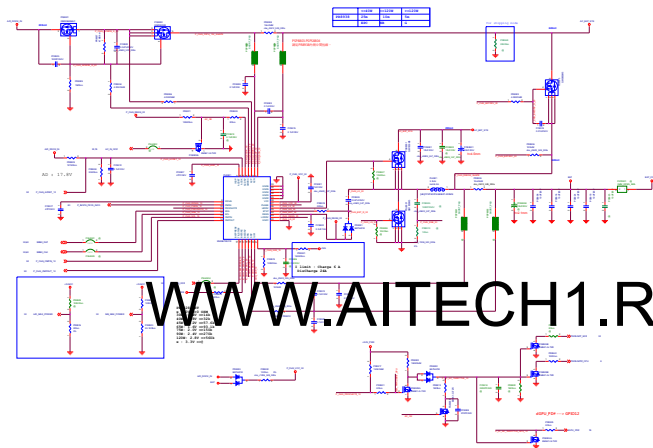
## 20151204 Modify



WWW.AITECH1.RU



ASUS	Project Name	XS420P/VRV
Time	1	PW_LOAD_SWITCH
Author	Project	Engineer
Version	1.0	1.0

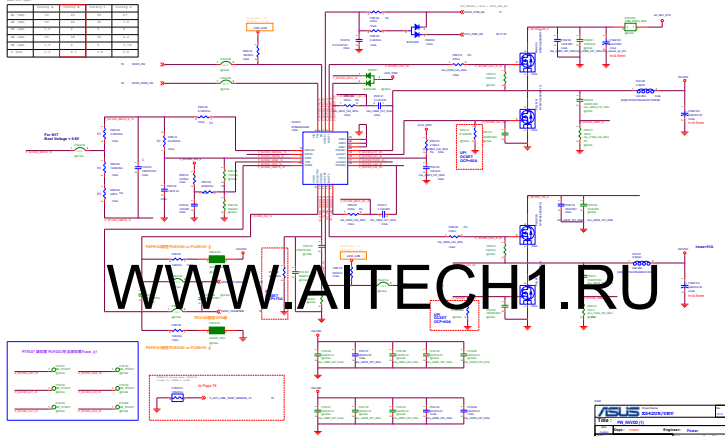


Address Selection Table

Address	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215	1216	1217	1218	1219	12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Pin 1-16: GND

Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin 1-16: GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

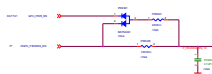
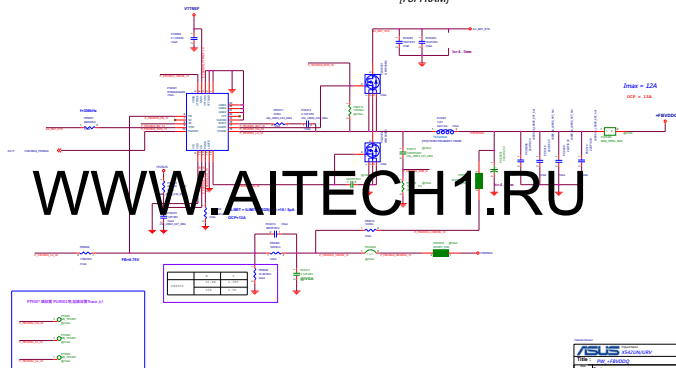


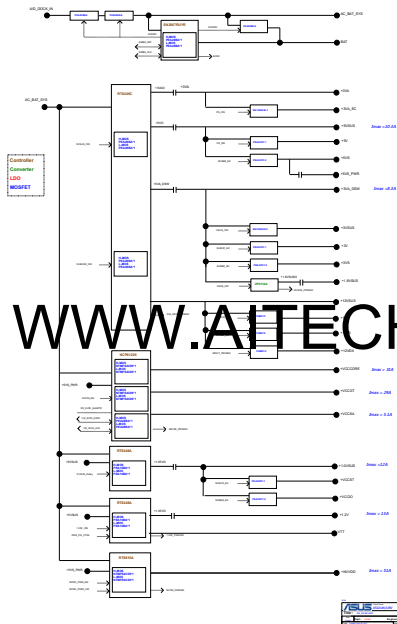
WWW.AITECH1.RU

ASUS	
Model: ROG STRIX Z690E-A	Revision: 1.0
Date: 2021.12.15	Author: ASUS
Engineer: ASUS	Checker: ASUS
Reviewer: ASUS	Approver: ASUS

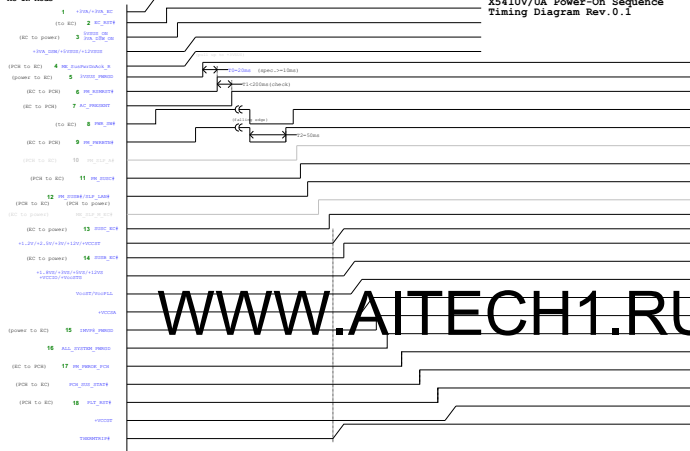
### 23 And 25 Truth Table

State	Pin7(S1)	Pin8(S1)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(S0-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+FBVDDQ  
[For FRAM]





X541UV/UA Power-On Sequence  
Timing Diagram Rev.0.1

# DC-IN Mode

1  $\rightarrow PWR\_VDDIN\_RC$   
(to RC) 2 RC\_RSTN

(RC to power) 3  $VDDIN\_ON$   
 $PWR\_VDDIN\_ON$

$\rightarrow PWR\_VDDIN\_VDDIN\_RC$

(PCR to RC) 4  $PM\_PWRVDDIN\_N$   
(power to RC) 5  $VDDIN\_PWRVDD$

(RC to PCR) 6  $PM\_PWRVDDIN$

(RC to PCR) 7  $RC\_PWRVDDIN$

(to RC) 8  $PWR\_VDDIN$

(RC to PCR) 9  $PM\_PWRVDDIN$

(PCR to RC) 10  $PM\_VDDIN\_N$

(PCR to RC) 11  $PM\_VDDIN$

12  $PM\_VDDIN\_VDDIN\_N$   
(PCR to RC) (PCR to power)

(RC to power) 13  $VDDIN\_RC$

$\rightarrow VDDIN\_VDDIN\_VDDIN\_VDDIN$

(RC to power) 14  $VDDIN\_VDDIN$

$\rightarrow VDDIN\_VDDIN\_VDDIN\_VDDIN$

$\rightarrow VDDIN\_VDDIN\_VDDIN\_VDDIN$

(power to RC) 15  $VDDIN\_PWRVDD$

16  $VDDIN\_PWRVDD$

(RC to PCR) 17  $PM\_PWRVDDIN$

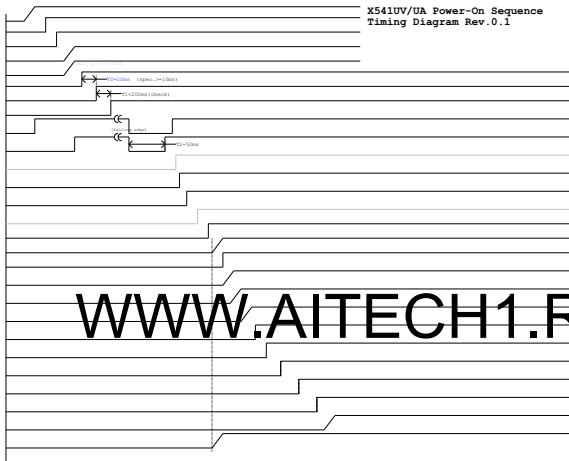
(PCR to RC)  $PCR\_PWRVDDIN$

(PCR to RC) 18  $PCR\_PWRVDDIN$

$\rightarrow VDDIN$

$VDDIN\_VDDIN$

## X541UV/UA Power-On Sequence Timing Diagram Rev.0.1



[illegible]